DETAILED ACTION

This final action is in response to the amendment filed on 03/12/2010. Claims 4, 16, & 27-36 are pending and have been considered as follows.

Examiner Note

The examiner has not issued a 35 U.S.C. 101 rejection for Claim 1 at this point in time as the applicants' Specification provides support for "a fault analysis apparatus," which is comprised of hardware, performing the method as claimed in Claim 1. However, the examiner recommends incorporating claim language amendments to clarify this detail. That is, the applicants should include amendments that would better clarify the method as performed by "a fault analysis apparatus." For example:

Claim 4 (Currently Amended) A fault analysis method, performed by a fault analysis apparatus, of presuming a fault location of a semiconductor IC comprising:

applying, by the fault analysis apparatus, a power supply voltage to said semiconductor IC;...

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 4, 16, & 27-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Su et al. ("Transient power supply current monitoring - A New test method for CMOS VLSI circuits") in view of Beasley et al. ("iDD pulse response testing applied to complex CMOS ICs") in view of Sakaguchi (US-5949798).

Claims 4, 16, & 27:

Su et al. disclose a fault analysis method of presuming a fault location of a semiconductor IC, a fault analysis apparatus configured to presume a fault location of a semiconductor IC, and a fault analysis apparatus configured to presume a fault location of semiconductor IC comprising,

- "applying a power supply voltage to said semiconductor IC" (i.e. "…This new method involves utilizing the dynamic power supply current, iDDT, as a window of observability into the switching behavior of a VLSI circuit. Using iDDT to detect IC defects… We use the transient power supply current as indicative of such switching…") [page 24 column 1];
- "supplying a test pattern sequence having a plurality of test patterns to said semiconductor IC" (i.e. "…We have developed design-for-iDDT-testability (DFIT) procedures that help exploit the use of iDDT. A partitioning algorithm is employed such that the switching behavior of every single gate input can be monitored

individually…Depending on the input pattern, the iDDT response can be the result of switching of more than one gate…test vectors are generated…test patterns (test vector pairs)…") [page 27 column 1, page 29 column 2, page 30 column 2, page 34 column 1];

- "the fault location list includes one or more locations of components in said IC" (i.e. "…Partitioning…For general multilevel circuit structures iDDT testability involves partitioning of the circuit; not in the traditional sense of decoupling voltage nodes but in the sense of separately observing the iDDT response of each module. We refer to this type of partitioning as pseudo-partitioning. Pseudo-partitioning only involves distribution of power to the circuit in such a way that the iDDT effects resulting from circuit defects can be isolated from those resulting from normal circuit switching…fault isolation circuitry for each pseudo-partition (see Section 4.2)…") [page 30 columns 1-2];
- "the electrical potentials at the one or more locations are expected to change once the test pattern sequence is supplied" (i.e. "…In general, the faulty iDVr responses took the shape of one of the following: Type 1. A flat waveform with a small current pulse (usually the pulse magnitude is half as that of the defect-free iDD T pulse), or Type 2. A waveform with a period proportional to that of the trigger square waveform. Examples of the two types of faulty iDDT responses can be directly derived from the AVDD responses shown in the lower portion of both graphs in Figure 13. Recall from Section 3 that iDDT is directly proportional to the transient portion of AVDD since we used a 1 Kilo-Ohm resistive drop between the supply source and the supply input of the circuits under test. In general, the defect-free iDVr response is represented by a current pulse while the circuit is changing states…") [page 35 column 2];

- "measuring a time integral of a transient power supply current generated on said semiconductor IC in accordance with the change of said test pattern" (i.e. "…A waveform with a period proportional to that of the trigger square waveform. Examples of the two types of faulty iDDT responses can be directly derived from the AVDD responses shown in the lower portion of both graphs in Figure 13…") [page 35 column 2];
- "determining whether said transient current shows abnormality or not" (i.e. "…In general, the faulty iDVr responses took the shape of one of the following: Type 1. A flat waveform with a small current pulse (usually the pulse magnitude is half as that of the defect-free iDD T pulse), or Type 2. A waveform with a period proportional to that of the trigger square waveform…Typically, the current pulse in the defect-free iDDT response is due to a temporary PWR to GND path created while a circuit is making a state transition. In a circuit with a source/drain open defect, the temporary PWR to GND path could be cut for a specific input vector pair…There are 12 built-in single floating gate opens among the three IC's that were designed. A total of 8 of these defects were detected by the logic transition test…") [page 35 column 2, page 37 column 1];
- "presuming a fault location out of said fault location list based on said test pattern sequence" (i.e. "…Typically, the current pulse in the defect-free iDDT response is due to a temporary PWR to GND path created while a circuit is making a state transition. In a circuit with a source/drain open defect, the temporary PWR to GND path could be cut for

a specific input vector pair…There are 12 built-in single floating gate opens among the three IC's that were designed. A total of 8 of these defects were detected by the logic transition test…") [page 37 column 1];

- "the transient power supply current shows abnormality and said fault location list" (i.e. "…There are 12 built-in single floating gate opens among the three IC's that were designed. A total of 8 of these defects were detected by the logic transition test…") [page 35 column 2, page 37 column 1];
- "said transient power supply current is determined to be abnormal in a case that the time integral of said transient power supply current is over a predetermined value in said step of determining" (i.e. "…In general, the faulty iDVr responses took the shape of one of the following: Type 1. A flat waveform with a small current pulse (usually the pulse magnitude is half as that of the defect-free iDD T pulse), or Type 2. A waveform with a period proportional to that of the trigger square waveform…Typically, the current pulse in the defect-free iDDT response is due to a temporary PWR to GND path created while a circuit is making a state transition. In a circuit with a source/drain open defect, the temporary PWR to GND path could be cut for a specific input vector pair…There are 12 built-in single floating gate opens among the three IC's that were designed. A total of 8 of these defects were detected by the logic transition test…") [page 35 column 2, page 37 column 1];
- "the fault location corresponds to at least one of an open defect or a delay fault" (i.e. "…In a circuit with a source/drain open defect…A total of 8 of these defects were detected by the logic transition test…") [page 37 column 1];

but, they do not explicitly disclose,

- "storing a fault location list for the test pattern sequence," although Sakaguchi does suggest storage for test pattern sequences and other data, as recited below;
- "said presuming comprises: deleting analysis points corresponding to the test pattern sequence where the transient power supply current does not show abnormality from analysis points corresponding to the test pattern sequence where the transient power supply current shows abnormality," although Beasley et al. do suggest determining which circuit tests result in a fault, as recited below;
- "presuming a remaining analysis point out of the analysis points corresponding to the test pattern sequence where the transient power supply current shows abnormality to be a fault location," although Beasley et al. do suggest determining which circuits are defective based on the completed fault tests, as recited below;

however, Beasley et al. do disclose,

- "...Table 2 SME scoring of the iDDPRT Time-Domain Tests for the SA3865. The time-domain tests performed up to this point for the SA3865 show limited success for detecting functional failures. While the success rate (85.7%) is promising, it is not satisfactory for full device screening in a manufacturing environment. Four functional failures were misclassified as "Good." On the other hand, 11 of the 15 functional failures were successfully removed from the test lot without requiring additional expensive test time. The time-domain tests for the SA3865 provided the following useful results: the iDDPRT test shows good promise for detecting functional failures...the iDDPRT time domain analysis technique used in this test was not suitable for detecting IDDQ

failures…Since this analysis is described by a simple equation, and can be performed rapidly, it has the potential to be implemented in a production test program…" [page 34];

whereas, Sakaguchi does disclose,

- "…In a CMOS integrated circuit, only a very slight leak current flows as the supply current except for transient currents in transistor switching operations. This character of the CMOS integrated circuit can be utilized to detect troubles therein. A trouble is detected on the basis of a large current, which is not the transistor switching current or the leak current… FIG. 12 shows another prior art example of the trouble detection system. In this case, a tester 1 applies a test pattern from a test pattern storage unit 3 to a CMOS integrated circuit 4 under test, and the supply current at this time is detected in a current detection unit 6. A checking unit 7 checks for a trouble in the circuit 4 from the result of the detection or observation. FIG. 13 shows a method of current measurement carried out in an IC checking system for checking electric characteristics of ICs (integrated circuits)…" [column 1 lines 14-20, 30-35 & FIG's 1, 4, 6, & 8-12 illustrate pattern storage unit and program storage unit];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to include, "storing a fault location list for the test pattern sequence" and "said presuming comprises: deleting analysis points corresponding to the test pattern sequence where the transient power supply current does not show abnormality from analysis points corresponding to the test pattern sequence where the transient power supply current shows abnormality" and "presuming a remaining analysis point out of the analysis points corresponding to the test pattern sequence where the transient power supply current shows abnormality to be a

fault location," in the invention as disclosed by Su et al. since it would have been expected by on of ordinary skill in the art to store test patterns and information on which circuits/components are defect for the purposes of providing a formulated and controlled test analysis that can be modified/adjusted as necessary to provide more verbose test results.

Claims 28-30:

Su et al., Beasley et al., and Sakaguchi disclose a fault analysis method of presuming a fault location of a semiconductor IC, a fault analysis apparatus configured to presume a fault location of a semiconductor IC, and a fault analysis apparatus configured to presume a fault location of semiconductor IC, as in Claims 4, 16, & 27 above, their combination further comprising,

- "the semiconductor IC is a CMOS IC" (i.e. "…CMOS ICs…") [Beasley et al. page 32].

Claims 31-33:

Su et al., Beasley et al., and Sakaguchi disclose a fault analysis method of presuming a fault location of a semiconductor IC, a fault analysis apparatus configured to presume a fault location of a semiconductor IC, and a fault analysis apparatus configured to presume a fault location of semiconductor IC, as in Claims 28-30 above, their combination further comprising,

- "the time integral of said transient power supply current is a sum of integrals of transient currents that flow in logic gates of the CMOS IC" (i.e. "…The observed (oi) iDDPRT generated power-on transient current for each of the ICs in the SA3865 test lot were then compared to the expected (q) power-on transient current response using Eq. 1…") [page 33].

Claims 34-36:

Su et al., Beasley et al., and Sakaguchi disclose a fault analysis method of presuming a fault location of a semiconductor IC, a fault analysis apparatus configured to presume a fault location of a semiconductor IC, and a fault analysis apparatus configured to presume a fault location of semiconductor IC, as in Claims 28-30 above, their combination further comprising,

- "the fault location list includes one or more locations of components which are connected to a common power supply" (i.e. "…the gates in a circuit share one or more common power supply rail…") [page 29 column 2 & page 30 columns 1-2].

Response to Arguments

3. Applicant's arguments with respect to claims 4, 16, & 27-36 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Oscar Louie whose telephone number is 571-270-1684. The examiner can normally be reached Monday through Friday from 8:30 AM to 5:00 PM. The examiner can also be contacted via E-mail to schedule a telephone discussion at OSCAR.LOUIE@USPTO.GOV.

If attempts to reach the examiner by telephone or E-mail are unsuccessful, the examiner's supervisor, Nasser Moazzami, can be reached at 571-272-4195. The fax phone number for Formal or Official faxes to Technology Center 2400 is 571-273-8300.

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06/08/2010

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